1.   (Currently amended) A programmable interconnect structure <u>to couple a first node to a</u> <u>second node</u> for an integrated circuit comprising:

a pass-gate fabricated on a substrate layer to electrically connect (a) <u>said</u> first node to (a) <u>said</u> second node; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating said first and second nodes and connecting said first and second nodes <u>by changing data stored in said memory bit</u>.

2.   (Original) The structure of claim 1, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

3.   (Original) The structure of claim 1, wherein said memory element is comprised one of a volatile and a non volatile memory element.

4.   (Original) The structure of claim 1, wherein said memory element is selected from one of a fuse link, an anti-fuse capacitor, an SRAM cell, a DRAM cell, a metal optional link, an EPROM cell, an EEPROM cell, a flash cell, a ferro-electric element, an optical element and a magnetic element.

5.   (Currently amended) The <u>structure of claim 1, wherein said programmable method is</u> <u>further comprised</u> of claim 1, further comprising:

providing a configuration access to alter data in <u>the</u> stored memory element; and

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generating a control signal from said memory element; and

controlling the polarity of said control signal by said stored memory bit polarity; and

coupling said control signal to the gate electrode of said pass-gate; and

selecting one of turning said ~~pass-gate~~ pass-gate off to isolate said first node from said second

node, and turning said pass-gate on to connect said first node to second node.

6.   (Currently amended) A programmable <u>interconnect structure to couple a first node to a</u>

<u>second node</u> ~~buffer structure~~ for an integrated circuit comprising:

~~a first and a second terminal; and~~

<u>a power voltage and a ground voltage; and</u>

a ~~programmable~~ pull-up ~~and a programmable pull-down~~ circuit coupled between said ~~first~~ <u>power</u>

<u>voltage</u> and <u>said</u> second <u>node</u> ~~terminals~~; and

<u>a pull-down circuit coupled between said ground voltage and said second node; and</u>

<u>a programmable circuit coupled to said first node and to each of said pull-up and pull-down</u>

<u>circuits; and</u>

a configuration circuit including at least one memory element coupled to said ~~pull-up and pull-~~

~~down circuits; and~~ <u>programmable circuit, wherein altering the data in said at least one</u>

<u>memory element provides a programmable method of:</u>

<u>decoupling said first node from second node by deactivating both said pull-up and pull-</u>

<u>down circuits; and</u>

<u>coupling said first node to second node compelled by activating said pull-up and pull-</u>

<u>down circuits.</u>

~~a programmable method to select between isolating said first terminal from second terminal by~~

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deactivating said pull-up and pull-down circuits, and coupling said first terminal to second terminal by activating said pull-up and pull-down circuits.

7.   (Currently amended) The structure of claim 6, wherein said first ~~terminal~~ <u>node</u> is coupled to an output from a logic block, said logic block comprising one of fixed logic and programmable logic.

8.   (Currently amended) The structure of claim 6, wherein said second ~~terminal~~ <u>node</u> is <u>coupled to</u> a wire comprising a capacitive load.

9.   (Original) The structure of claim 6, wherein said configuration circuit is comprised of one memory element.

10.   (Currently amended) The structure of claim 6, wherein said programmable method of ~~isolating terminals~~ <u>decoupling said first node from said second node</u> is further comprised of isolating said ~~first and~~ second <u>node</u> ~~terminals~~ from both pull-up and pull-down circuits.

11.   (Currently amended) The structure of claim 6, wherein said programmable method of coupling <u>said first node to said second node</u> is further comprised of transferring a signal at said first ~~terminal~~ <u>node</u> to said second ~~terminal~~ <u>node</u> by the method comprised of:

  deactivating said pull-down circuit and activating said pull-up circuit to provide a source

    current <u>from said power voltage</u> to said second ~~terminal~~ <u>node;</u> and

  deactivating said pull-up circuit and activating said pull-down circuit to provide a sink

current ~~to~~ from said second ~~terminal; and~~ node to said ground voltage.

~~adjusting said source and sink current strengths to provide a buffered signal at said~~

~~second terminal.~~

12.   (Currently amended) The structure of claim 11, wherein said source current and sink current strength is adjusted by sizing said pull-up and pull-down circuit transistors respectively, and wherein adjusting said source and sink current strengths provides a restored signal at said second node.

13.   (Currently amended) The structure of claim 6, wherein the programmable circuit is further ~~comprising a pull-up circuit~~ comprised of:

an inverter comprising an input and an output; and

a programmable method of selecting one of said first ~~terminal~~ node and ~~(a)~~ said ground voltage

as the input of ~~(an)~~ said inverter; and

the output of said inverter coupled to said pull-up circuit.

~~a pull-up device controlled by output of said inverter coupled between a power supply and said~~

~~second terminal.~~

14.   (Currently amended) The structure of claim 6, wherein the programmable circuit is further ~~comprising a pull-down circuit~~ comprised of:

an inverter comprising an input and an output; and

a programmable method of selecting one of said first ~~terminal~~ node and ~~(a)~~ said power voltage as

the input of ~~(an)~~ said inverter; and

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<u>the output of said inverter coupled to said pull-down circuit.</u>

~~a pull-down device controlled by output of said inverter coupled between said second terminal and a ground supply.~~

15.   (Currently amended) The structure of claim 6, further comprised of:

said pull-up and pull-down circuits, each comprising a pass-gate fabricated on a substrate layer; and

said configuration circuit comprising ~~a transistor~~ <u>said at least one memory element</u> fabricated substantially above said substrate layer.

16.   (Currently amended) The structure of <u>claim 15</u> ~~claim 6~~, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

17.   (Original) The structure of claim 6, wherein said memory element is comprised one of volatile and non volatile memory element.

18.   (Original) The structure of claim 6, wherein said memory element is selected from one of a fuse link, an anti-fuse capacitor, an SRAM cell, a DRAM cell, a metal optional link, an EPROM cell, an EEPROM cell, a flash cell, a ferro-electric element, an optical element and a magnetic element.

19.   (Currently amended) The structure of claim 6, wherein said programmable ~~method~~ <u>circuit</u>

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further comprises:

~~fabricating~~ one or more programmable pass-gates and logic transistors <u>located</u> on a substrate layer; and

~~fabricating~~ one or more configuration access transistors and memory transistors <u>located</u> on thin-film layers substantially above said substrate layer; and

~~coupling~~ one or more control signals <u>generated</u> from said thin film memory elements <u>coupled</u> to gate electrodes of said pass-gates; and

~~providing~~ user access <u>circuitry</u> to change said thin film memory data via said thin film access transistors.

20.   (Currently amended) <u>The structure of claim 19, wherein the</u> ~~The method of claim 19,~~ ~~further comprising fabricating~~ configuration circuits <u>are located above the substrate layer by</u> using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket NMOS Vt P- implant;

applying PMOS Vt mask & N- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

applying P2 mask & etching P2;

applying blanket LDN N- implant;

applying LDP mask & P- implant;

depositing a spacer oxide and etching the spacer oxide;

applying blanket N+ implantation of NMOS G/S/D;

applying P+ mask & implanting PMOS G/S/D;

depositing Nickel;

salicidizing the Nickel on the G/S/D regions & interconnect;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

21.   (Currently amended) <u>The structure of claim 19, wherein the</u> ~~The method of claim 19,~~

~~further comprising fabricating~~ configuration circuits <u>are located above the substrate layer by</u>

using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket Gated-NFET Vt N- implant;

applying Gated-PFET Vt mask & P- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

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applying blanket P+ implantation of Gated-NFET Gate;

applying N+ mask & implanting Gated-PFET Gate;

applying P2 mask & etching P2;

applying blanket LDN N implant (Gated-NFET LDD);

applying LDP mask & P implant (Gated-PFET LDD);

depositing a spacer oxide and etching the spacer oxide;

depositing Nickel;

salicidizing the Nickel on exposed P1 and P2;

salicidizing P1 completely;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

22.   (Currently amended) A programmable interconnect ~~bi-directional data wire~~ structure to

couple a first node to a second node for an integrated circuit comprising:

a wire having a first end and a second end ~~end, said wire comprising a capacitive load~~; and

a first programmable interconnect structure ~~buffer structure, said structure~~ as in claim 6, the first

node of said first claim 6 structure coupled to said first node and the second node of said

first claim 6 structure ~~comprising an input and an output, said output~~ coupled to said first

end of wire; and

a second programmable interconnect structure ~~buffer structure, said structure~~ as in claim 6, the

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first node of said second claim 6 structure coupled to said second node and the second

node of said second claim 6 structure ~~comprising an input and an output, said output~~,

coupled to said second end of wire; and

~~a programmable method of selecting between said first buffer transmitting data and said second~~

~~buffer tri-stated, and said second buffer transmitting data and said first buffer tri-stated.~~

a programmable method of coupling said first node to the wire by coupling said first claim 6

structure, and coupling said second node to the wire by coupling said second claim 6

structure; and

a programmable method of decoupling said first and second nodes from the wire by decoupling

both of said first and second claim 6 structures.

23.   (Original) The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said first end of wire

and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

24.   (Original) The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said second end of

wire and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

25.   (Currently amended) The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said <u>first node</u> ~~input~~

of first programmable buffer structure and an external output; and

a programmable method of selecting at least one of said external outputs to connect to said first

node buffer input.

26. (Currently amended) The structure of claim 22 claim 25 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said second node

input of second programmable buffer structure and an external output; and

a programmable method of selecting at least one of said external outputs to connect to said

second node buffer input.

27. (Currently amended) A bi-directional bus structure programmable interconnect structure

to couple a plurality of first nodes to a plurality of second nodes for an integrated circuit

comprising:

a first side comprising each of said first nodes wherein said structure where said bus originates

and a second side comprising each of said second nodes wherein said structure where

said bus terminates; and

a plurality of programmable interconnect structures as stated bi-directional wire structures, each

structure as in claim 22, each said claim 22 structure further comprising:

the first node of claim 22 structure coupled to a first node at said first side with said

structure wire having the first end at said first side; and

the second node of claim 22 structure coupled to a second node at said second side with

said structure wire having the second end at said second side.

said wire extending from said first side to said second side; and

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~~said first buffer comprising a first side input at said first side; and~~

~~said second buffer comprising a second side input at said second side.~~

28.   (Currently amended) The structure in claim 27 further comprising:

a plurality of inputs <u>and a plurality of interconnect structures as in claim 1</u>, each <u>said</u> input connecting to (~~a~~) <u>the</u> first node of ~~a plurality of interconnect structures, each structure as in claim 1,~~ <u>said claim 1 structure,</u> the second ~~nodes of said plurality of structures~~ <u>node of</u> said claim 1 structure connecting to <u>the wire first end of a said claim 22 structure</u> ~~each of said wires in said bus~~ at said first side; and

a plurality of outputs <u>and a plurality of interconnect structures as in claim 1</u>, each <u>said</u> output connecting to (~~a~~) <u>the</u> first node of ~~a plurality of interconnect structures, each structure as in claim 1,~~ <u>said claim 1 structure,</u> the second ~~nodes of said plurality of structures~~ <u>node of</u> said claim 1 structure connecting to <u>a first node at said first side</u> ~~each of said first side inputs of said first side buffers~~; and

a programmable method of selecting at least one of said inputs and <u>at least</u> one of said outputs to connect to <u>said first side</u> ~~each of said wires in said bus~~.

29.   (Currently amended) The structure in claim 27 further comprising:

a plurality of inputs <u>and a plurality of interconnect structures as in claim 1</u>, each <u>said</u> input connecting to (~~a~~) <u>the</u> first node of ~~a plurality of interconnect structures, each structure as in claim 1,~~ <u>said claim 1 structure,</u> the second ~~nodes of said plurality of structures~~ <u>node of</u> said claim 1 structure connecting to <u>the wire second end of a said claim 22 structure</u> ~~each of said wires in said bus~~ at said second side; and

a plurality of outputs <u>and a plurality of interconnect structures as in claim 1</u>, each <u>said</u> output

connecting to (a) <u>the</u> first node of ~~a plurality of interconnect structures, each structure as~~

~~in claim 1,~~ <u>said claim 1 structure,</u> the second ~~nodes of said plurality of structures~~ <u>node of</u>

<u>said claim 1 structure</u> connecting to <u>a second node at said second side</u> ~~each of said second~~

~~side inputs of said second side buffers~~; and

a programmable method of selecting at least one of said inputs and one of said outputs to connect

to <u>said second side</u> ~~each of said wires in said bus~~.

30.   (Currently amended) The structure of claim 6, further comprising a pass-gate coupled

between said first and second ~~terminals~~ <u>nodes,</u> wherein:

said configuration circuit is further coupled to said pass-gate; and

said programmable method further comprises activating said pass-gate when <u>said</u>

<u>programmable circuit decouples the nodes</u> ~~buffer is tri-stated~~, and deactivating

said pass-gate when said <u>programmable circuit couples the nodes</u> ~~buffer is~~

~~activated~~.

31.   (Currently amended) The structure of claim 30, wherein said first ~~terminal~~ <u>node</u> is

coupled to an input/output from a logic block, said logic block comprising one of fixed logic and

programmable logic.

32.   (Currently amended) The structure of claim 30, wherein said second ~~terminal~~ <u>node</u> is a

wire comprising a capacitive load.

33.   (Original) The structure of claim 30, wherein said configuration circuit is comprised of one memory element.

34.   (Currently amended) The structure of claim 30, wherein said programmable <u>circuit couples the nodes</u> ~~method comprising an activated buffer~~ is further comprised of transferring a signal at said first ~~terminal~~ <u>node</u> to said second ~~terminal~~ <u>node</u> by the method comprised of:

      deactivating said pull-down circuit and activating said pull-up circuit to provide a source current to said second ~~terminal~~ <u>node</u>; and

      deactivating said pull-up circuit and activating said pull-down circuit to provide a sink current to said second ~~terminal~~ <u>node</u>; and

      adjusting said source and sink current strengths to provide a buffered signal at said second ~~terminal~~ <u>node</u>.

35.   (Currently amended) The structure of claim 30, further comprised of:

said pass-gate fabricated on a substrate layer; and

said pull-up and pull-down circuit comprising a pass-gate fabricated on said substrate layer; and

said configuration circuit comprising <u>the memory element</u> ~~a transistor~~ fabricated substantially above said substrate layer.

36.   (Original) The structure of claim 30, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

37.   (Currently amended) A <u>programmable interconnect</u> ~~bi-directional data wire~~ structure <u>to</u>

couple a first node to a second node for an integrated circuit comprising:

a wire having a first end and a second end ~~end, said wire comprising a capacitive load~~; and

a first programmable interconnect structure ~~buffer structure, said structure~~ as in claim 30, the first node of said first claim 30 structure coupled to said first node and the second node of said first claim 30 structure ~~comprising an input and an output, said output~~ coupled to said first end of wire; and

a second programmable interconnect structure ~~buffer structure, said structure~~ as in claim 30, the first node of said second claim 30 structure coupled to said second node and the second node of said second claim 30 structure ~~comprising an input and an output, said output~~, coupled to said second end of wire; and

~~a programmable method of selecting between said first buffer transmitting data and said second buffer tri-stated, and said second buffer transmitting data and said first buffer tri-stated.~~

a programmable method of coupling said first node to second node by activating the first claim 30 structure pass-gate and deactivating the second claim 30 structure pass-gate, or by deactivating the first claim 30 structure pass-gate and activating the second claim 30 structure pass-gate.

38.   (Currently amended) The structure of claim 30, wherein the programmable method ~~of claim 37,~~ further comprising:

providing a configuration access to alter data in stored memory element; and

generating complementary control signals from said memory element; and

controlling the polarity of said control signals by said stored memory bit polarity; and

coupling said complementary control signals to said pass-gate and pull-up and pull-down

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circuits; and

selecting between turning said ~~pass gate~~ pass-gate off and activating said pull-up and pull-down circuits, and turning said pass-gate on and deactivating said pull-up and pull-down circuits.

39. (Currently amended) The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said first end of wire and an external input; and

a programmable method of selecting ~~at least one of~~ said external inputs to connect <u>or disconnect</u> to said wire.

40. (Currently amended) The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said second end of wire and an external input; and

a programmable method of selecting ~~at least one of~~ said external inputs to connect <u>or disconnect</u> to said wire.

41. (Currently amended) The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said <u>first node</u> ~~input of first programmable buffer structure~~ and an external input/output; and

a programmable method of selecting ~~at least one of~~ said external input/outputs to connect <u>or</u> <u>disconnect</u> to said first ~~buffer input~~ <u>node</u>.

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42.   (Currently amended) The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said ~~second node input of second programmable buffer structure~~ and an external input/output; and

a programmable method of selecting ~~at least one of~~ said external input/outputs to connect <u>or disconnect</u> to said second ~~buffer input~~ <u>node</u>.

43.   (Currently amended) A ~~method of forming a~~ programmable interconnect structure for an integrated circuit comprising:

    ~~fabricating~~ one or more pass-gates on a substrate layer to electrically connect two ~~points~~ <u>nodes</u>; and

    ~~selectively fabricating~~ either a memory circuit or a conductive pattern <u>in lieu of said memory circuit</u> substantially above said pass-gates to control a portion of said pass-gates; and

    ~~fabricating~~ an interconnect and routing layer substantially above said ~~memory circuits~~ <u>pass-gates</u> to connect said pass-gates and one of said memory circuits and conductive ~~pattern.~~ pattern; and

    <u>a programmable method to select between isolating said first and second nodes and connecting said first and second nodes by changing data either in the memory circuits or in the conductive pattern.</u>

44.   (Currently amended) The ~~method~~ <u>structure</u> of claim 43, further comprised of ~~fabricating~~ a user configurable memory circuit on a thin film layer comprising one of fuse links, anti-fuse capacitors, SRAM, DRAM, metal optional links, EPROM, EEPROM, flash, ferro-electric,

optical and magnetic memory elements.

45.   (Currently amended) The ~~method~~ <u>structure</u> of claim 43, further comprised of said conductive pattern comprising ~~fabricating~~ hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire coupled to ground; and

a logic one memory output mapped to a hard wire coupled to power.

46.   (Currently amended) The ~~method~~ <u>structure</u> of claim 45, wherein a given configuration of said memory circuit and the corresponding conductive pattern have one or more substantially matching signal propagation delays for said structure.

47.   (Currently amended) The ~~method~~ <u>structure</u> of claim 43, further comprised of said conductive pattern comprising ~~fabricating~~ hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire coupled to ground; and

a logic one memory output mapped to a hard wire shorting drain to source of pass-gate controlled by said logic one memory element.

48.   (Currently amended) The ~~method~~ <u>structure</u> of claim 47, wherein a given configuration of said memory circuit operated at an elevated memory power supply voltage and the corresponding conductive pattern ~~have~~ <u>has</u> one or more substantially matching signal propagation delays ~~for said switch~~.